

(Fig. 1b I, 1b II, 1b III)

(Fig. 1c)

(Fig. 1d)

(Fig. 1f1, 1f2)

Fig. 1a

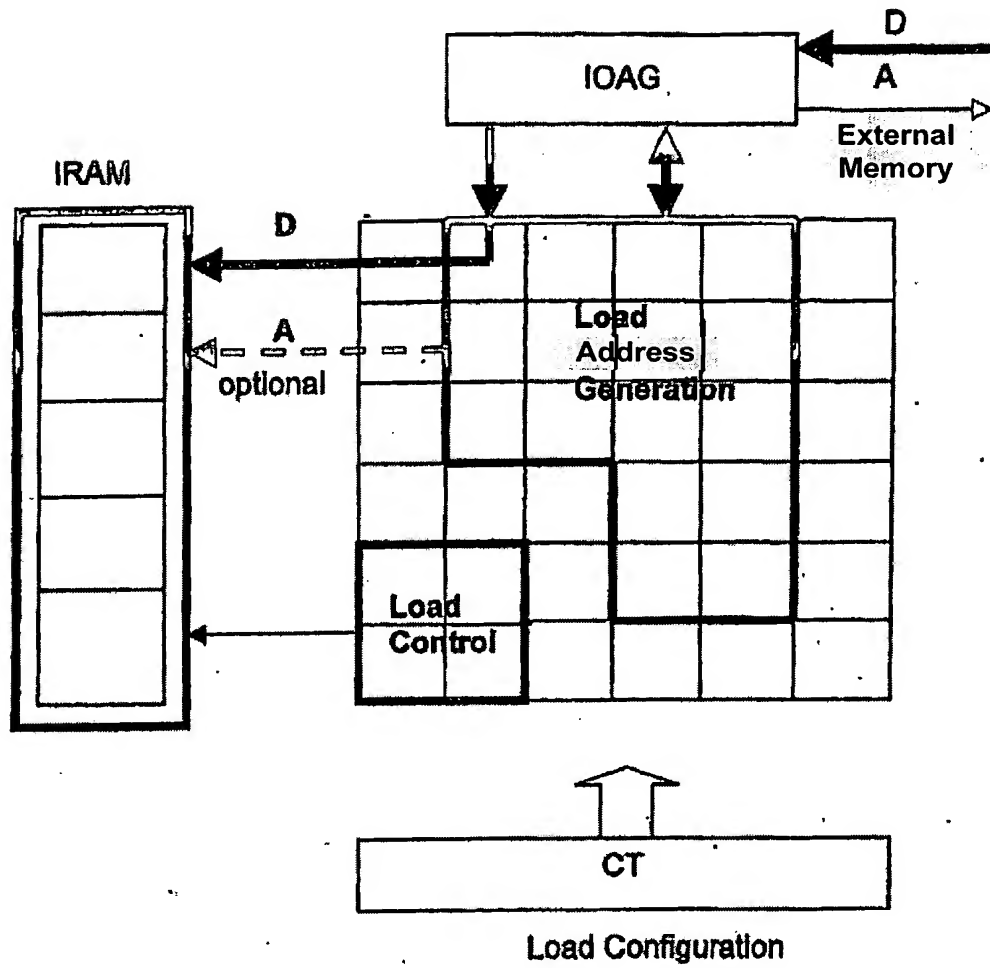


Fig. 1b I

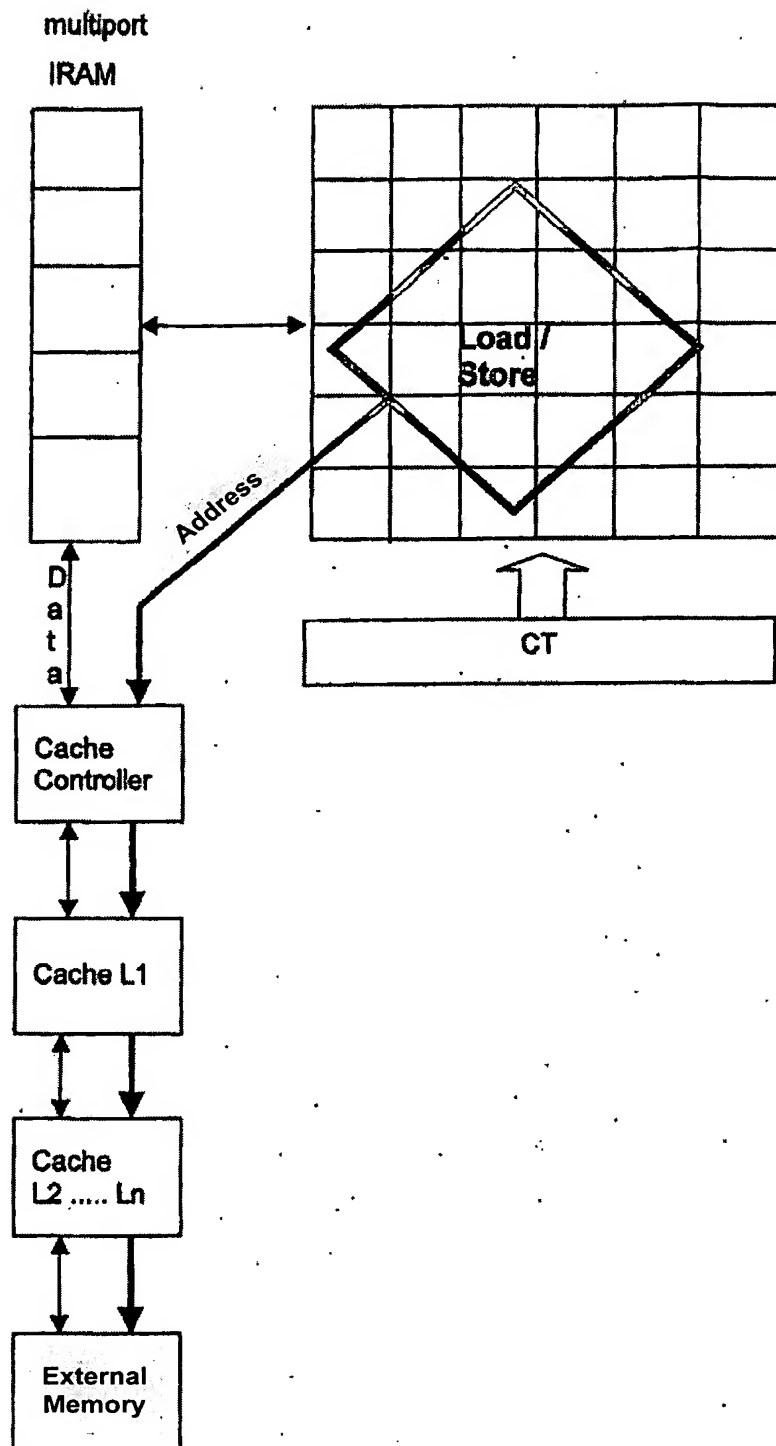


Fig. 1b II

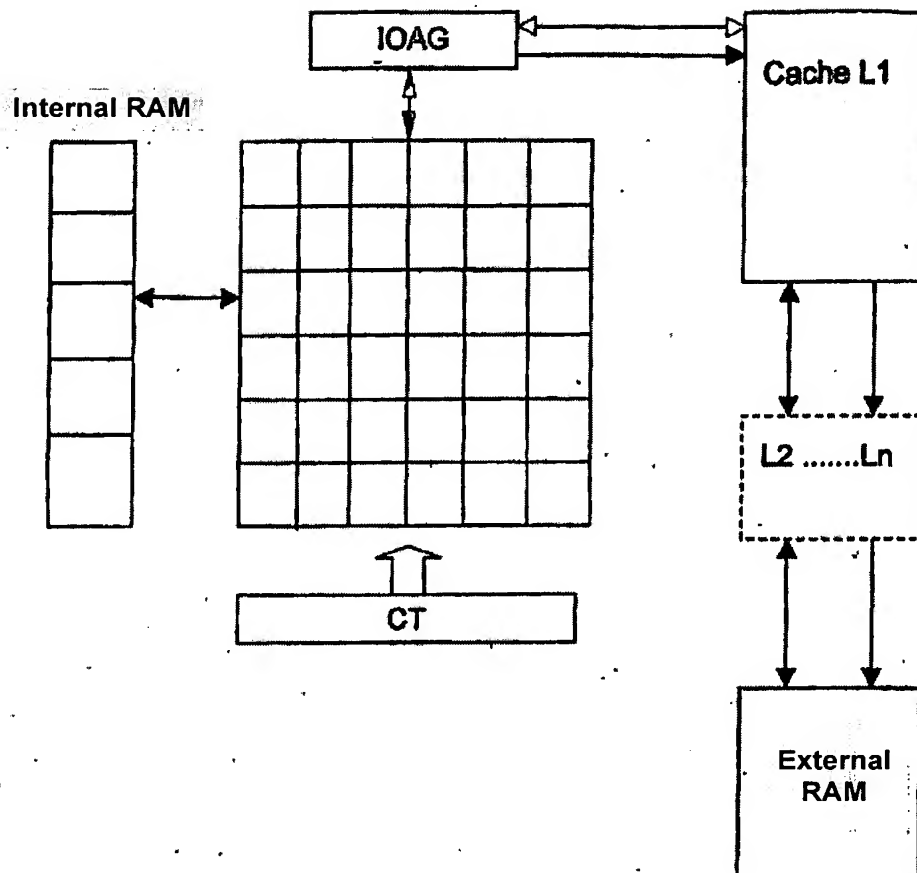


Fig. 1b III

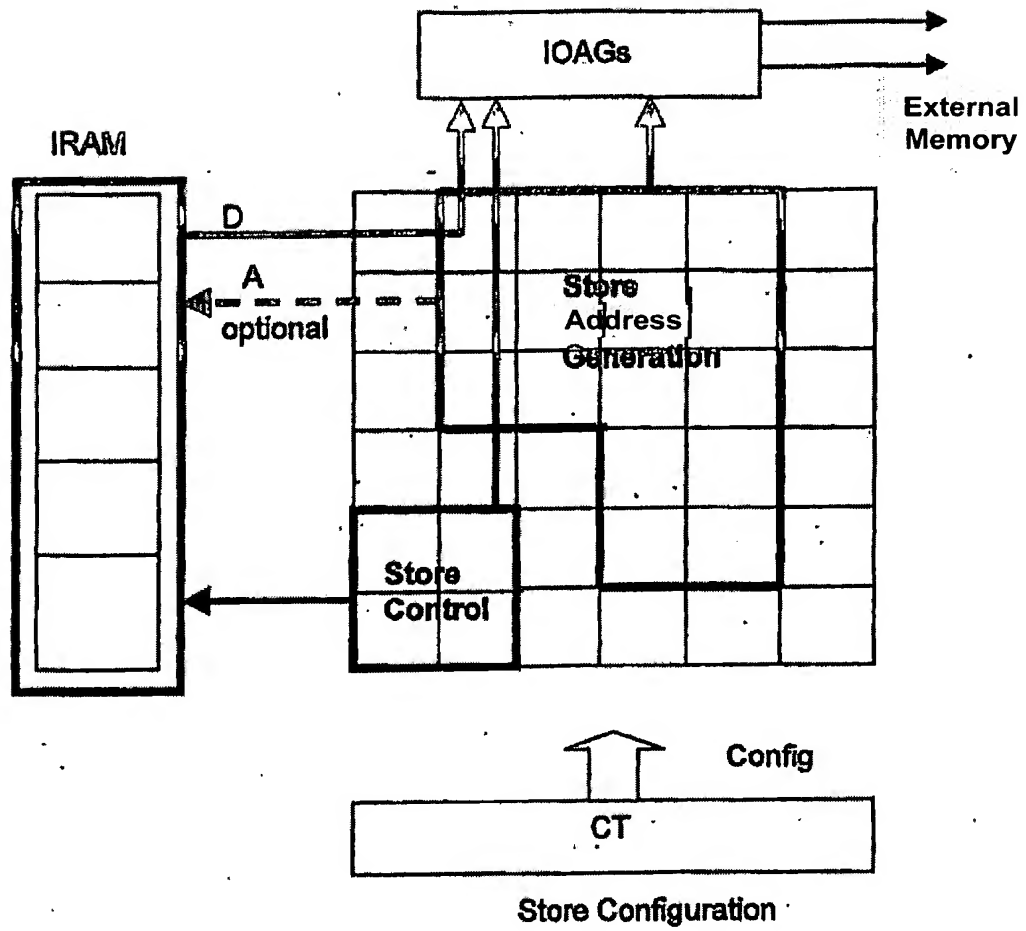


Fig. 1f1

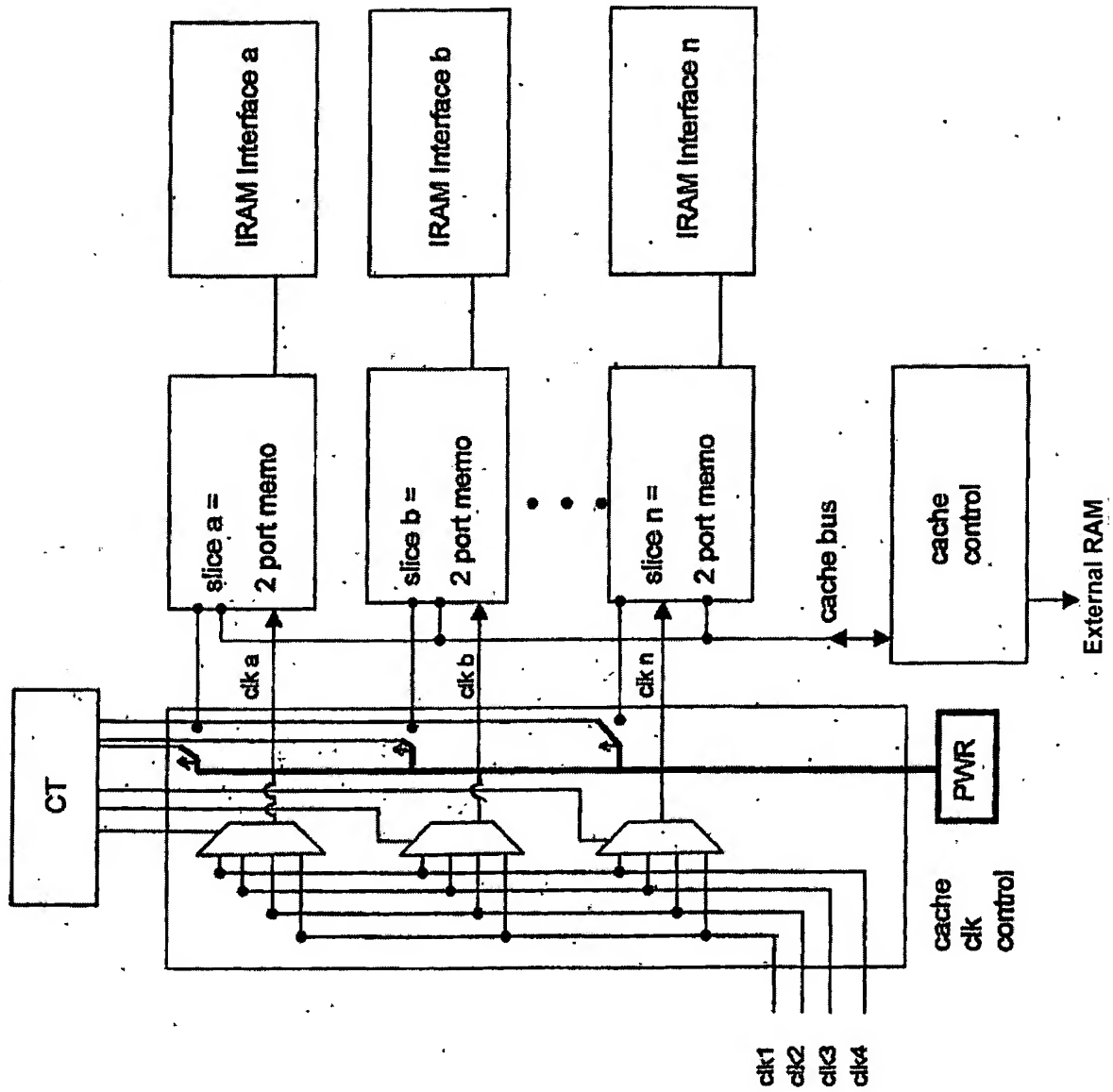
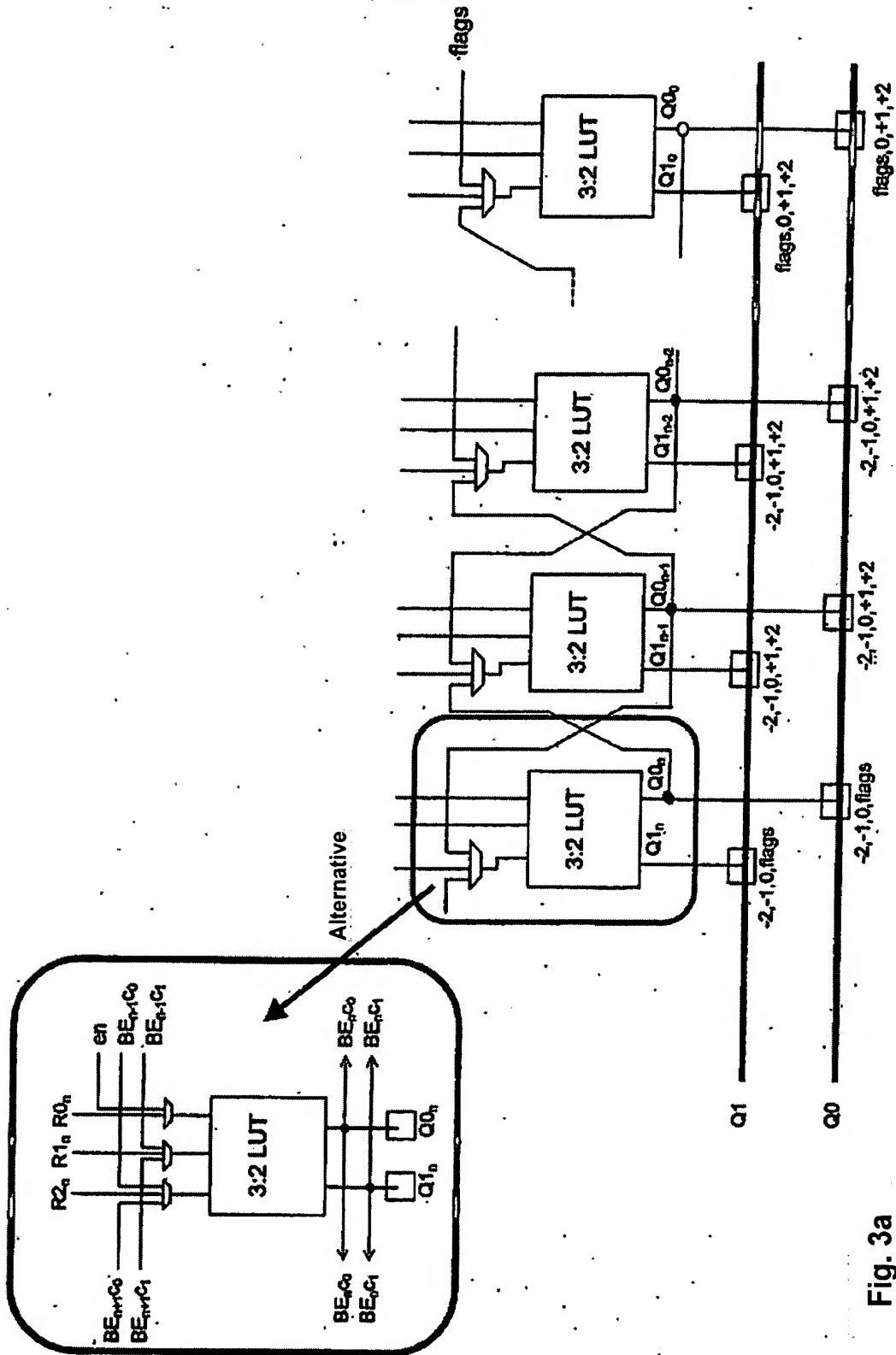
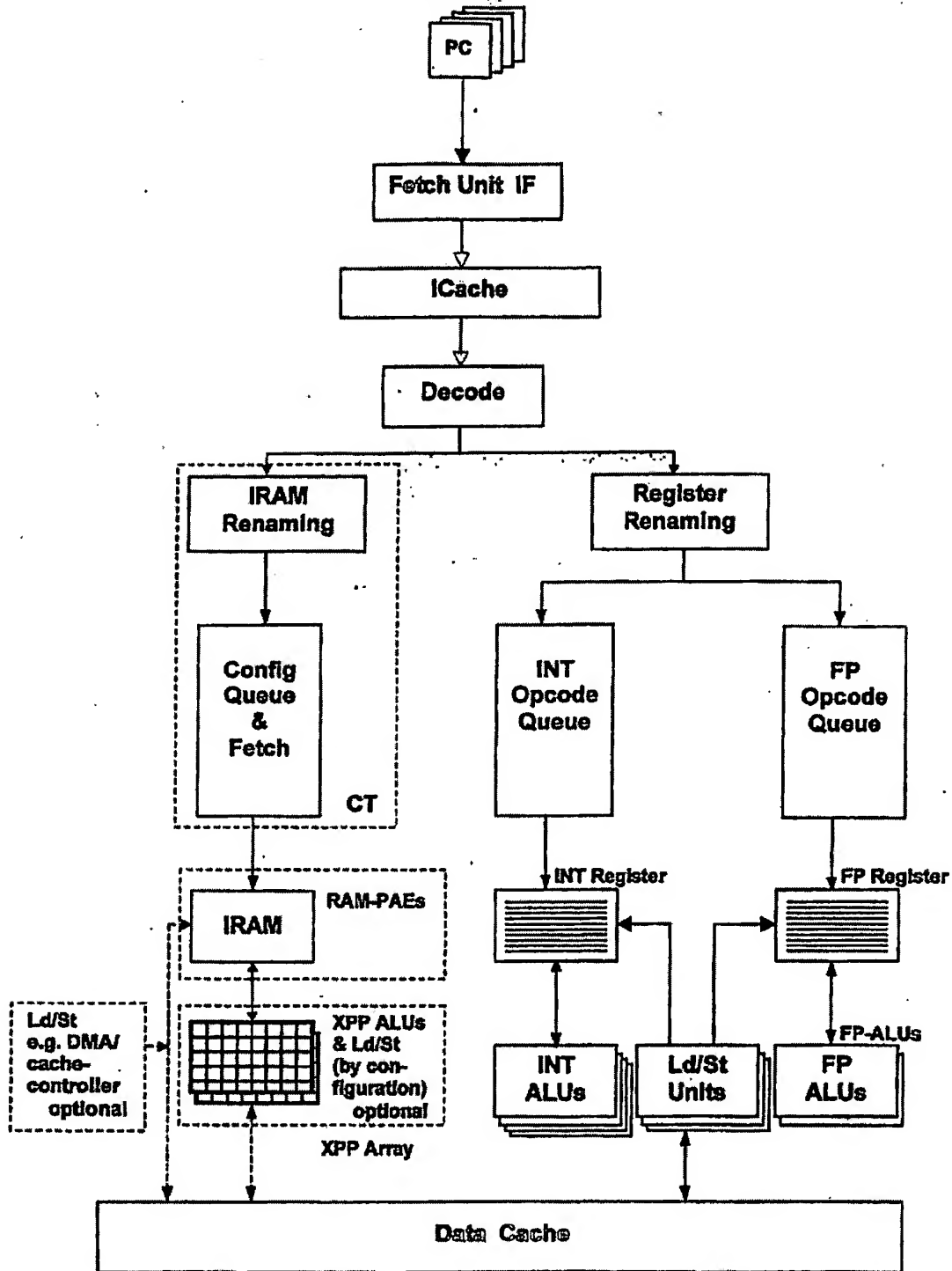


Fig. 2



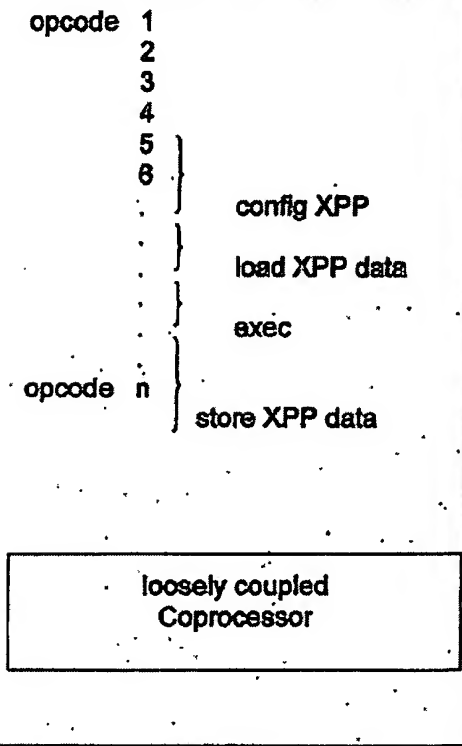


Possible Structure of an SMT Processor having
XPP Thread Resource

Fig. 4a

XPP in the Instruction Stream

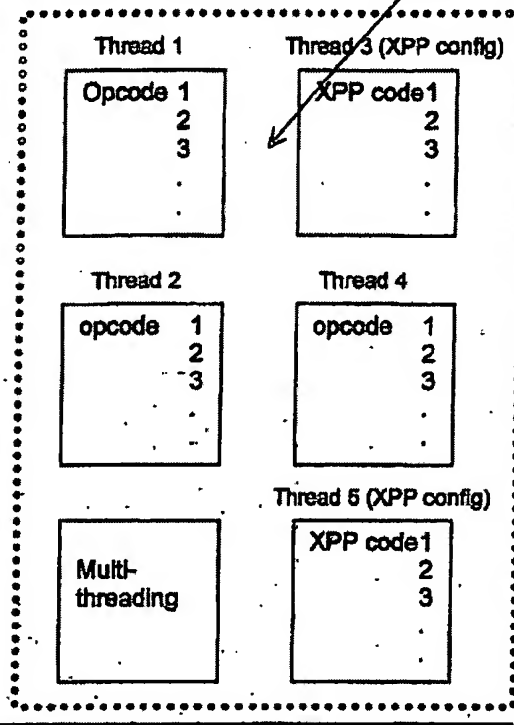
triggered by CPU commands



XPP as Thread Resource

The threads are partitioned and used by the scheduler

Fig. 6c



XPP in the Instruction Stream

triggered by XPP commands separated by the IF/ID slice

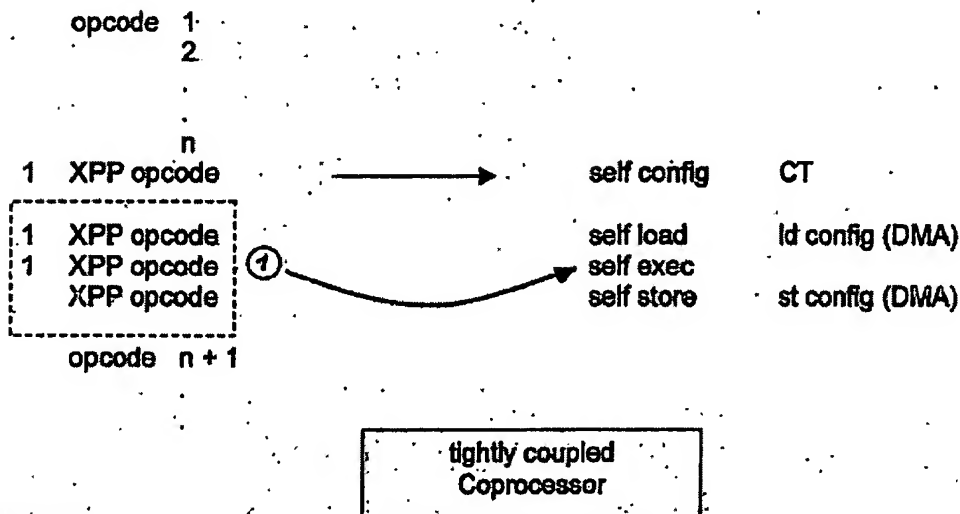


Fig. 6b